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APPLICATION FOR LETTERS PATENT
OF THE UNITED STATES

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TITLE OF INVENTION: METHOD FOR FORMING A TOP OXIDE WITH NITRIDE LINER

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

Patent Application
02P03330US (8055-147)

METHOD FOR FORMING A TOP OXIDE WITH NITRIDE LINER

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present disclosure relates to semiconductor devices, and more particularly to a method for forming a top oxide with a nitride liner.

2. Discussion of Prior Art:

Semiconductor memory devices such as dynamic random access memories (DRAM) typically include memory cells. These memory cells comprise storage nodes. These storage nodes can be formed within deep trenches etched into substrate of a semiconductor memory chip. The storage nodes can be accessed using an access transistor, which allows a charge to be stored in the storage node or retrieved from the storage node depending on a desired action, e.g., a read function or a write function. Electrical isolation of the storage node from a gate conductor can be important to the performance of the device.

A top trench oxide layer formed over the storage node provides electrical isolation between the storage node and gate conductor. Each storage node typically includes a polysilicon material that partially fills the deep trench. During

fabrication of the device, a recess can be formed at the top of the trench. An oxide, for example, silicon oxide, can be formed over the device including the polysilicon in the trench. Portions of the deposited oxide can be removed by planarizing the surface of the device and by recessing the oxide to leave an oxide layer at the bottom of the recess, for example, 5-50nm of material. This oxide layer is referred to as a trench top oxide or isolation.

Similar to the trench top oxide, a top oxide for vertical transistors provides electrical isolation. The top oxide isolates the gate conductor from the substrate. An electrical connection can be formed between the gate conductor wiring layer on the wafer surface and the vertical gate conductor in the trench. Methods for forming the top oxide typically involve complex process flows, which can add to the cost of manufacturing the DRAM devices. In addition, exposed arrays during processing can result in irregularities in the DRAM device affecting device performance.

Therefore, a need exists for a method for structuring a top oxide with a nitride liner having a reduced number of process steps and a protected stud during processing.

SUMMARY OF THE INVENTION

According to an embodiment of the present disclosure, a method for forming a top oxide for a vertical transistor device comprising a poly stud above a polysilicon fill in a deep trench and an isolation region in a portion of the deep trench, comprises forming an etch support nitride liner by low-pressure chemical vapor deposition over the poly stud, and forming a support polysilicon over a portion of the isolation trench outside of an array. The method further comprises depositing a top oxide over the vertical transistor device, forming a planarization coating over the top oxide, and opening the nitride stud, wherein the top oxide remains over a portion of the isolation trench.

The method further comprises forming a nitride cap above the poly-stud above a polysilicon fill in a deep trench.

Forming an etch support nitride liner further comprises forming implants.

The implants are formed in a well, a support device, or both the well and the support device.

The method further comprises performing a support gate oxidation prior to forming the support polysilicon, wherein the polysilicon stud is protected from the support gate oxidation by the etch support nitride liner.

Forming the support polysilicon further comprises depositing an etch array polysilicon over the memory device, applying an etch array mask over a portion of the etch array polysilicon, etching the etch array polysilicon, and exposing a pad oxide on the substrate.

Opening the polysilicon stud comprises depositing a planarization coating, etching the planarization coating with a selectivity to oxide of 1:1, and selective to polysilicon, wherein the polysilicon in the support is either high enough to clear the top oxide or, where the top oxide in the support can be removed by a mask.

Opening the polysilicon stud comprises an etch of the planarization coating, selective to oxide 1:1, wherein the etch has an endpoint upon the exposure of the polysilicon cap.

Opening the polysilicon stud comprises an oxide etch of the top oxide, planarization coating 1:>2, selective to polysilicon, having an endpoint upon the removal to the organic planarization coating. The method further comprises a timed etch oxide 1:1, removing a portion of the polysilicon cap.

According to an embodiment of the present disclosure, a method for forming a top oxide for a vertical transistor device comprises providing a substrate, and forming a storage node in the substrate comprising a deep trench filed with a doped polysilicon. The method further comprises forming a polysilicon

stud above the doped polysilicon in the deep trench, forming an isolation trench in an upper portion of the storage node and substrate, and forming a patterned etch support liner over a portion of the polysilicon stud, wherein the patterned etch support liner and the doped polysilicon fully encompass the polysilicon stud. The method comprises depositing a top oxide over the vertical transistor device, forming a planarization coating over the top oxide, and opening the stud to expose the polysilicon stud, wherein portions of the top oxide are preserved above the substrate and above the isolation trench.

Forming the isolation trench comprises forming a pad nitride over a portion of the deep trench memory device exposing a portion of the substrate and the polysilicon stud, and etching an isolation trench in the exposed portion of the substrate and the nitride stud. Forming the isolation trench further comprises filling the isolation trench with an insulated material, removing the pad nitride to expose the substrate, and performing an oxide deglaze.

Opening the nitride stud comprises etching the planarization coating with a selectivity to oxide of 1:1, and selective to polysilicon, wherein the polysilicon in the support is either high enough to clear the top oxide or, where the top oxide in the support can be removed by a mask.

Opening the polysilicon stud comprises an etch of the planarization coating, selective to oxide 1:1, wherein the etch has an endpoint upon the exposure of the polysilicon stud.

Opening the polysilicon stud comprises an oxide etch of the top oxide, planarization coating 1:>2, selective to polysilicon, having an endpoint upon the removal to the organic planarization coating. The method further comprises a timed etch oxide 1:1, removing a portion of the polysilicon stud.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the present invention will be described below in more detail, with reference to the accompanying drawings:

Figures 1A to 1C are a flow chart of a method according to an embodiment of the present disclosure;

Figure 2 is a diagram of a cross-section of a transistor according to an embodiment of the present disclosure;

Figure 3 is a diagram of a cross-section of a transistor according to an embodiment of the present disclosure;

Figure 4 is a diagram of a cross-section of a transistor according to an embodiment of the present disclosure;

Figure 5 is a diagram of a cross-section of a transistor according to an embodiment of the present disclosure;

Figure 6 is a diagram of a cross-section of a transistor according to an embodiment of the present disclosure;

Figure 7 is a diagram of a cross-section of a transistor according to an embodiment of the present disclosure;

Figure 8 is a diagram of a cross-section of a transistor according to an embodiment of the present disclosure;

Figure 9 is a diagram of a cross-section of a transistor according to an embodiment of the present disclosure;

Figure 10 is a diagram of a cross-section of a transistor according to an embodiment of the present disclosure; and

Figure 11 is a diagram of a cross section taken along cleave line A in Figure 10.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A top oxide process is needed for vertical transistors to isolate the gate conductor from the substrate and to form an electrical connection between a gate conductor wiring layer and the vertical gates. Isolation is important, because, among other reasons, the gate conductor is used at the same time as a gate electrode for planar transistors in the support region of the substrate. U.S. Patent Application No. 20020196651, filed June 22, 2001, entitled Memory Cell Layout with Double Gate Vertical Array Transistor, describes a method for top oxide formation by

deposition and planarization, and is incorporated herein by reference in its entirety.

The present disclosure provides an improved method for forming a top trench isolation layer over a storage node in a deep trench, wherein an array is covered by a nitride liner preventing out doping, and a stud is not exposed to a gate oxidation.

Referring to Figures 1A to 1C, a method for forming a top oxide over an isolation trench of a storage node comprises forming an isolation trench (IT), wherein the IT is filled and polished 101. The IT electrically isolates each active array region formed on each side of the deep trench. An oxide deglaze can be performed to remove contaminants and a pad nitride can be removed to expose the substrate 102. Array implants can be formed on the device 103. Optionally, a portion of the pad oxide can be removed 104, for example, by hydrofluoric acid (HF), and a layer of sacrificial oxide can be formed over the device 105. An etch support (ES) nitride liner can be deposited over the device 106. Optionally, an in situ steam generation (ISSG) oxidation can be performed to create an oxide layer to be structured by resist. The pattern in the oxide can be used for etching the ES nitride liner with high selectivity. The ES nitride liner can be masked 107, followed by an ES nitride liner etch to pattern the ES liner 108. Implants can be added to wells

and support devices as needed 109. Support devices include, for example, read/write/erase control circuits and decoders. A sacrificial oxidation strip can remove the layer of sacrificial oxide 110. Support gate oxidation 111 prepares the surface of the device for a support polysilicon. An etch array (EA) polysilicon can be deposited 112, followed by the application of an EA mask 113. The support polysilicon or EA polysilicon can be etched from the array (e.g., by block-mask) 114. An ES nitride etch (of the material deposited in 109) can expose the oxide on the substrate and IT by removing portions of the ES nitride liner 115. This can also be performed as a spacer-etch. Any desired array implants can be formed 116. A top oxide can be deposited 117.

An organic planarizing coating, e.g., an antireflective coating (ARC), can be deposited. The organic planarizing coating can be planarized 119. A reactive ion etch (RIE) of the coating layer, e.g., with a selectivity of 1:1 (organic coating to oxide), selective to polysilicon, can be performed to open the polysilicon stud 120, wherein the polysilicon in the support is high enough to clear the top oxide. Alternatively, a second ES mask can be used to remove the oxide on the polysilicon.

Referring now to Figure 2, a storage node 200 comprises a deep trench (DT) filed with polysilicon 201 formed in a substrate 202, an IT 203 is polished, for example, by chemical-

mechanical polish (CMP), to a pad nitride surface 204. A DT nitride cap 205 is above a portion of a spacer 206 and the polysilicon 201. The spacer 206 may be formed of nitride. The spacer 206 may be omitted. Also shown are the top trench oxide 207, the trench collar oxide 208, and a polysilicon 209 of the lower portion of the deep trench. The polysilicon 209 can be highly doped when deposited to form a buried strap (described with respect to Figure 11). A node dielectric 210 lines the lower portion of the deep trench. Techniques for forming the top trench oxide 207, the trench collar oxide 208, the polysilicon 209, and node dielectric 210 would be obvious to one of ordinary skill in the art.

An oxide deglaze is performed to remove contaminants. The pad nitride is removed to expose the pad oxide in the substrate, e.g., the p-well. Array implants can be formed on the device. Optionally, a portion of the pad oxide can be removed. A layer of sacrificial oxide can be formed over the device.

Referring to Figure 3, an ES liner 301 can be deposited over the device. Optionally, an ISSG oxidation can be performed to form a hardmask for structuring the ES liner 301. The ES liner can be masked, followed by an ES nitride liner etch to pattern the ES liner 301. The etch can be by, for example, RIE or using the oxide hardmask above with a hydrofluoric acid (HF)

etch. Implants can be added to wells and support devices as needed.

Referring to Figure 4, a sacrificial oxidation strip removes the layer of oxide (not shown) in the support. Support gate oxidation prepares the surface of the device for receiving a support polysilicon 401. An EA mask 402 can be applied.

Referring to Figure 5, the EA polysilicon 401 in the array can be etched, with a block mask. An EA nitride-etch can expose the pad oxide on the substrate 202 and isolation trench 203 by removing portions of the ES liner 301. This can also be performed as a spacer-etch. Any desired array implants can be formed. A top oxide 501 can be deposited.

An organic planarization coating 601, as shown in Figure 6, can be formed. The organic planarization coating 601 can be for example, an ARC.

Referring to Figure 7, an RIE of the ARC layer, e.g., with a selectivity to oxide of 1:1, and selective to polysilicon, can be performed to open the polysilicon stud 701, wherein the polysilicon in the support 401 is either high enough to clear the top oxide 501 or, where the top oxide in the support area can be removed by an ES mask. Alternatively, an RIE of the ARC layer 601, e.g., oxide 1:1, can be performed having an endpoint upon the exposure of the top oxide 501, as shown in Figure 8. An oxide etch of the top oxide 501 can be performed as shown in

Figure 9, e.g., ARC 1:>2, selective to polysilicon, having an endpoint upon the removal to the ARC layer 601. Further, a timed RIE oxide 1:1 can be performed, removing a portion of the top oxide 501 as shown in Figure 9. The RIE can be an oxide-etch selective to polysilicon 401 until the polysilicon stud 701 is free as shown in Figure 10.

Referring to Figure 11, a wordline/support gate stack is illustrated along the cleave line A shown in Figure 10 taken through an active array region on each side of the deep trench. A buried plate (not shown) forms one plate of the capacitor. A dielectric layer, formed of oxide or nitride, or a combination, lines the deep trench forming a node dielectric as shown in Figure 2. A trench collar oxide 208 is formed in the trench below the top trench oxide 207. Doped polysilicon 209 formed within a lower portion of the deep trench acts as a second plate. A buried strap 1101 is a lower junction, wherein the polysilicon 201 forms a gate between the buried strap 1101 and the upper junction 1106. The structure shown in Figure 11 can be manufactured given the unstructured gate stack of Figure 10 by known techniques. For example, by depositing a metal stack followed by a gate nitride layer, performing gate/mask structuring, and a spacer process. The spacer process forms a spacer around the wordline. More particularly, as shown in Figure 11, a wordline stack 1102 is deposited over the

polysilicon stud 701 and top oxide 501. The wordline stack 1102 is preferably a multi-layer stack of polysilicon and tungsten. The spacer 1103 encompasses the wordline 1102. Also shown are a transition region 1107 and a support isolation trench 1104 underlying a support gate stack 1105.

Having described embodiments for a system and method for forming a top oxide with a nitride liner, it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes may be made in the particular embodiments of the invention disclosed which are within the scope and spirit of the invention as defined by the appended claims.